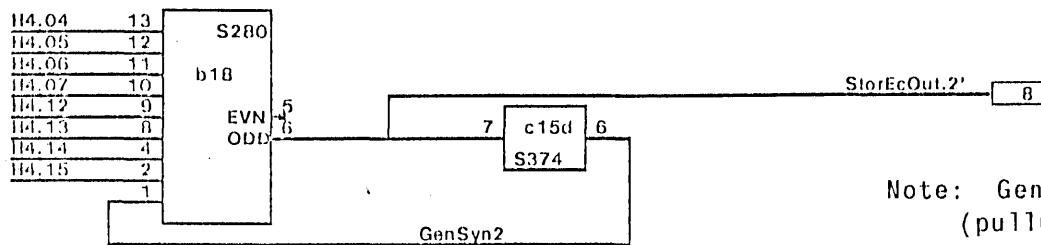
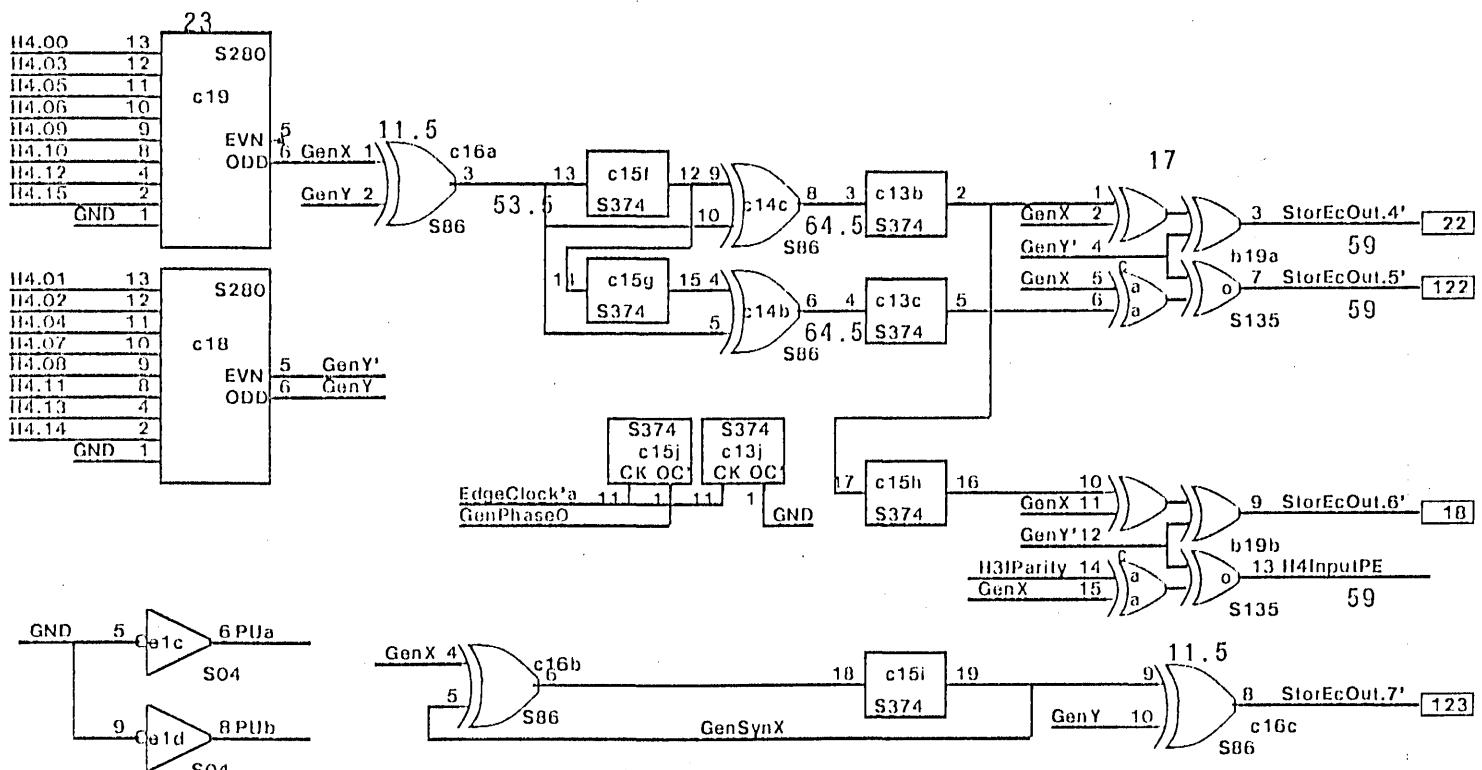
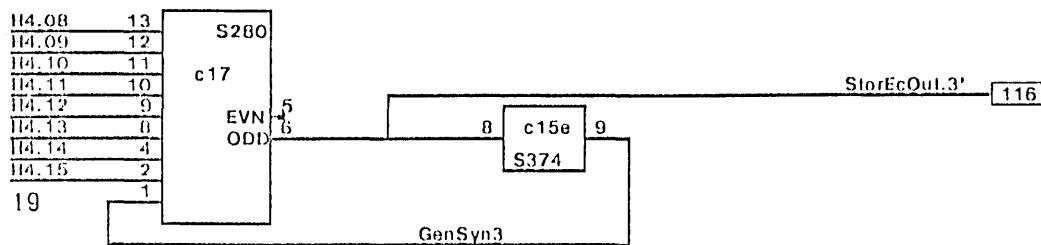


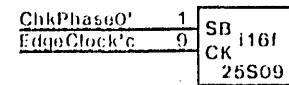
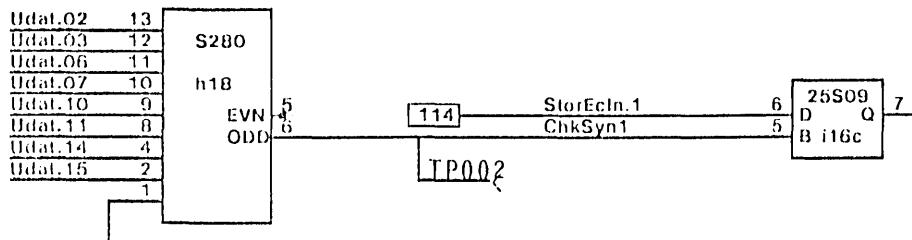
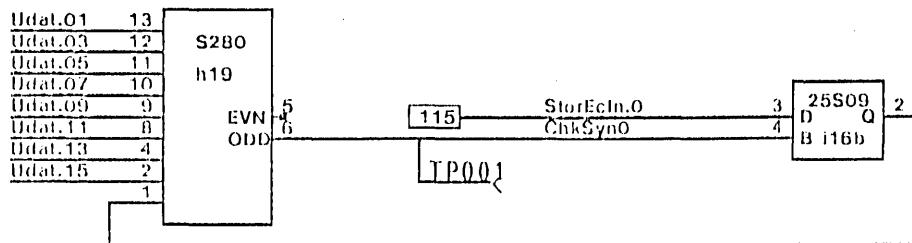
Note: Storage card inverts  
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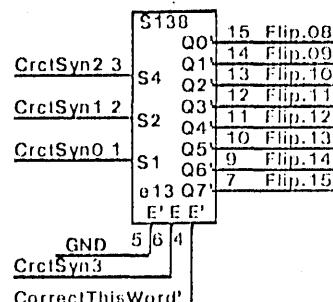
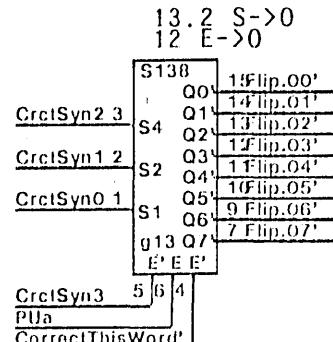
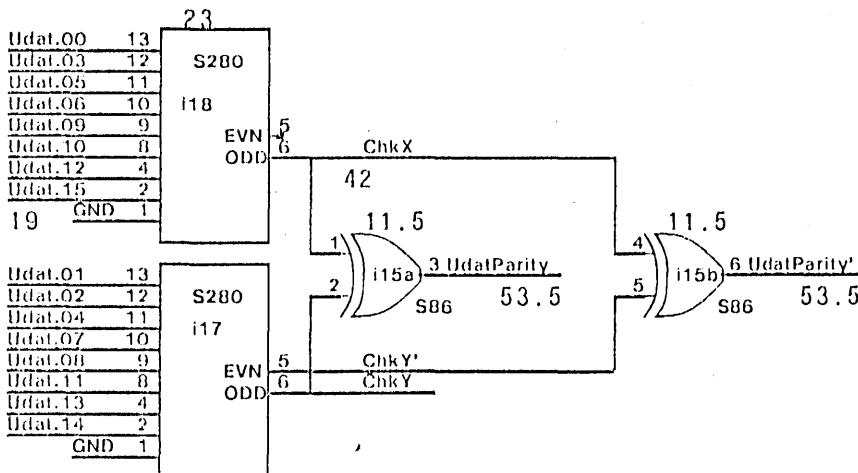
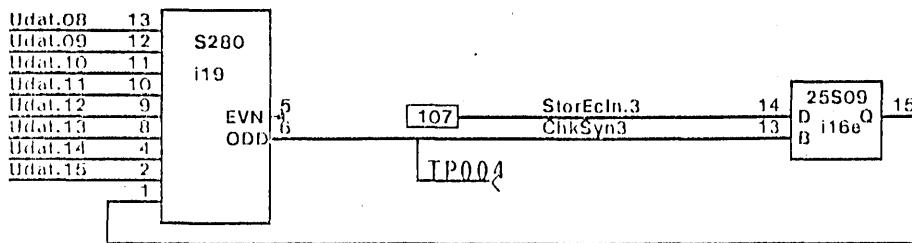
Note: GenPhase0 => GenSyn0,1,2,3,X =  
(pullups on page 12)



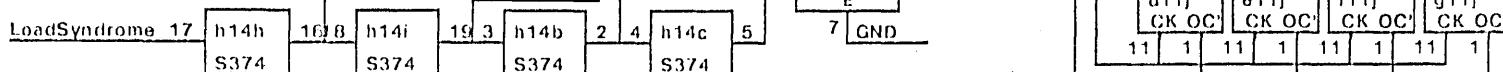
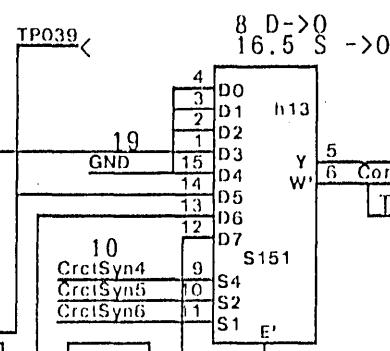
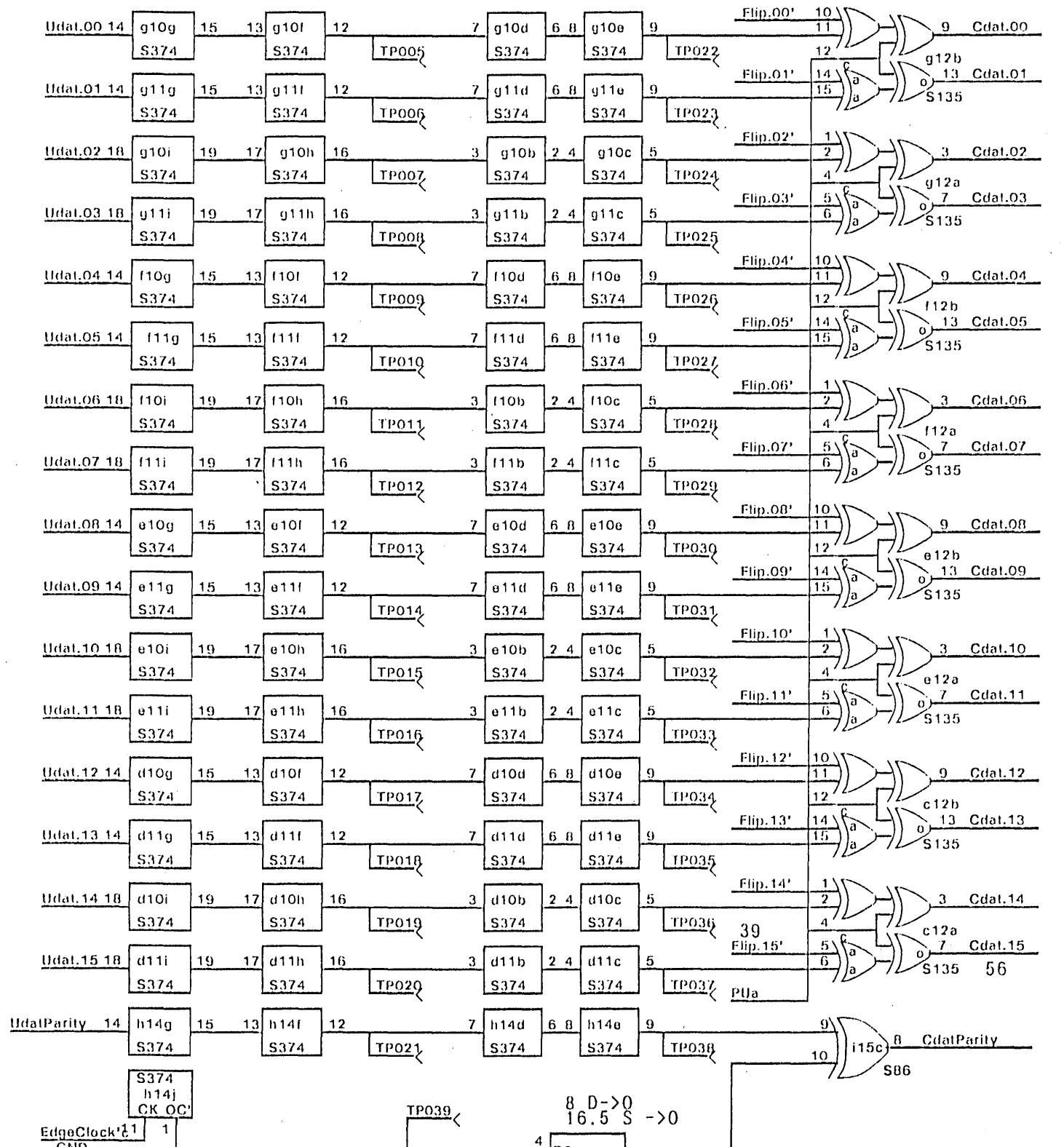
XEROX EOD	Project DO	Memory Control Error Correction Generator	File D0mem01.sil	Designer Thacker	Rev Gb	Date 7/18/80	Page 01
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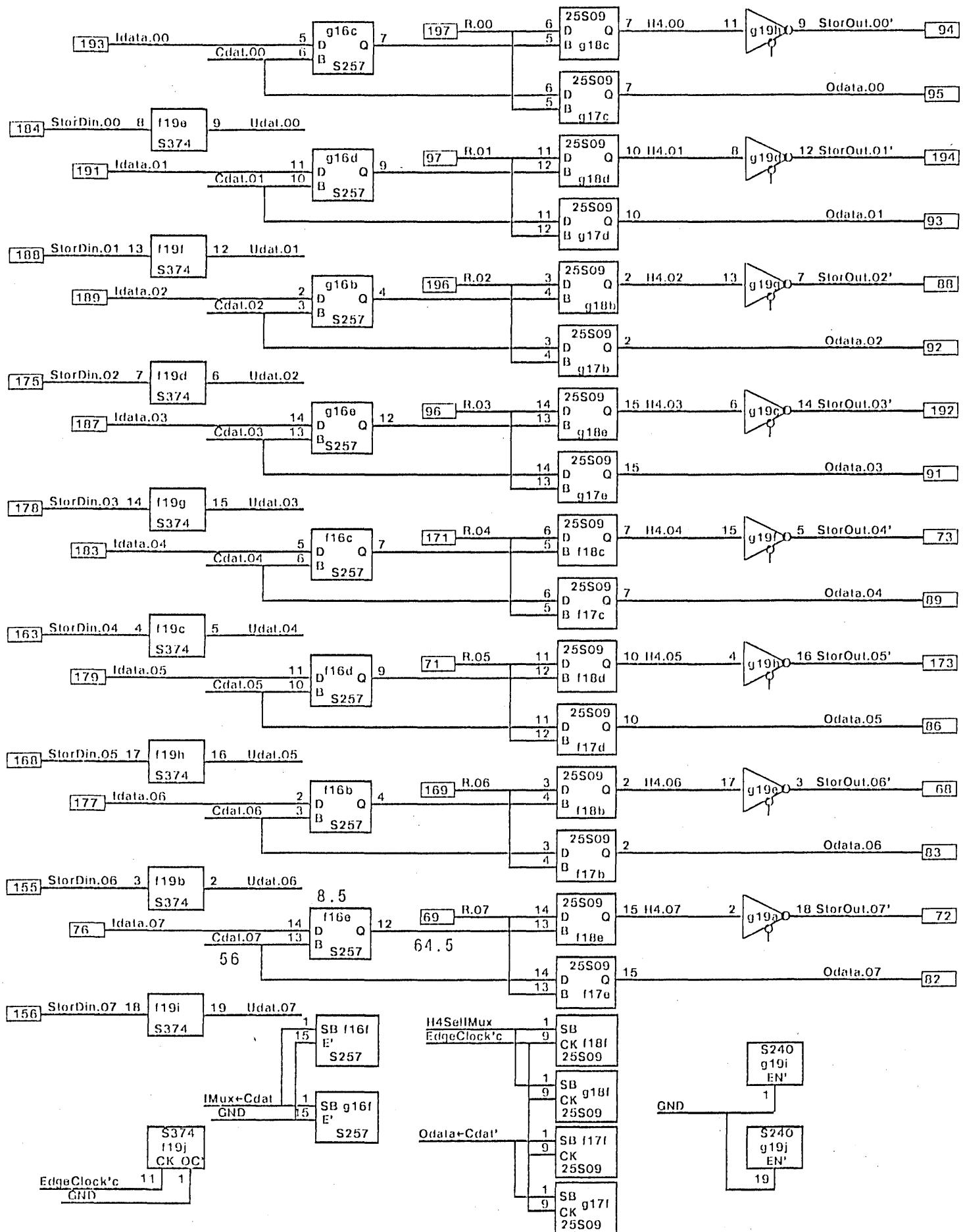


Note: Storage card inverts data and check bits

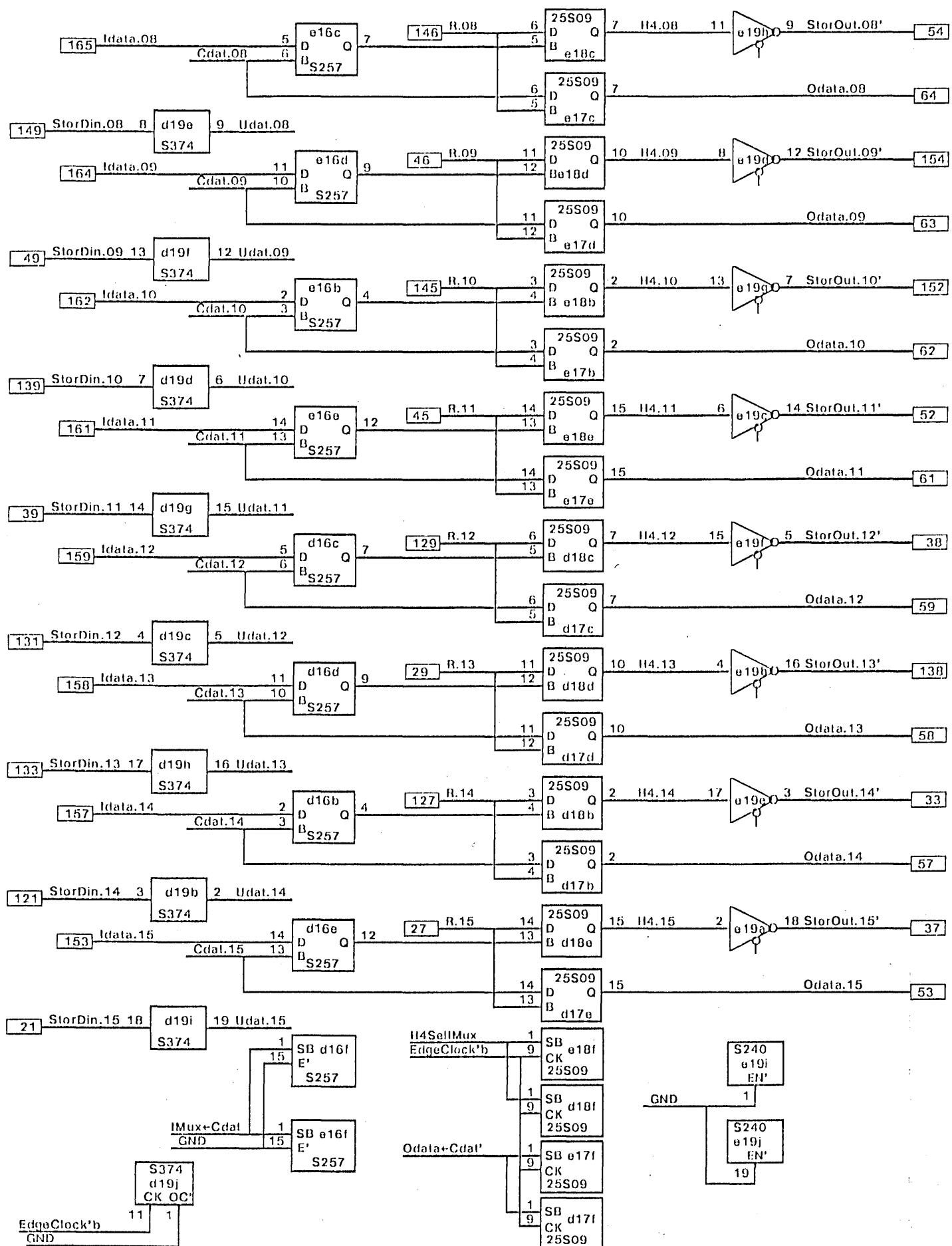


Note: Balance of checker is on pg. 6



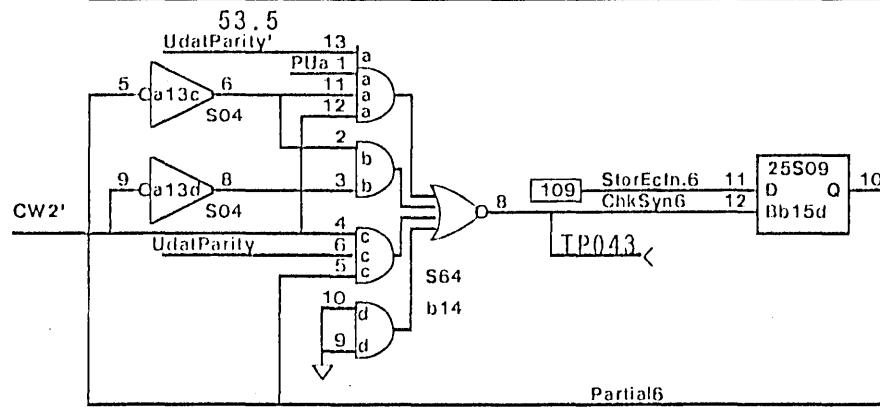
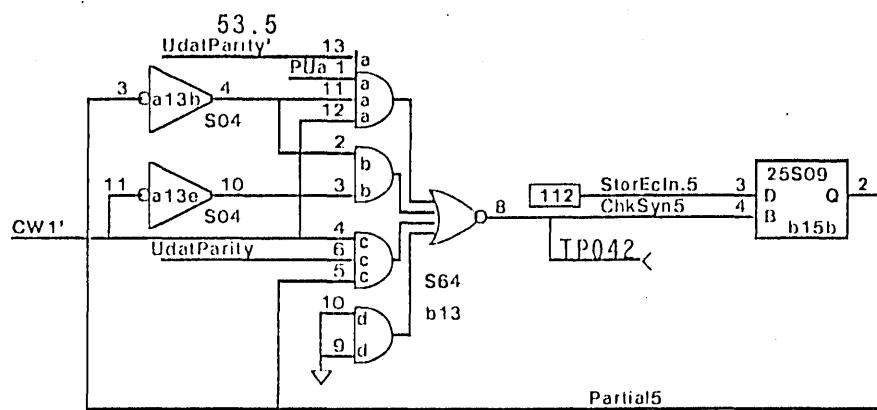
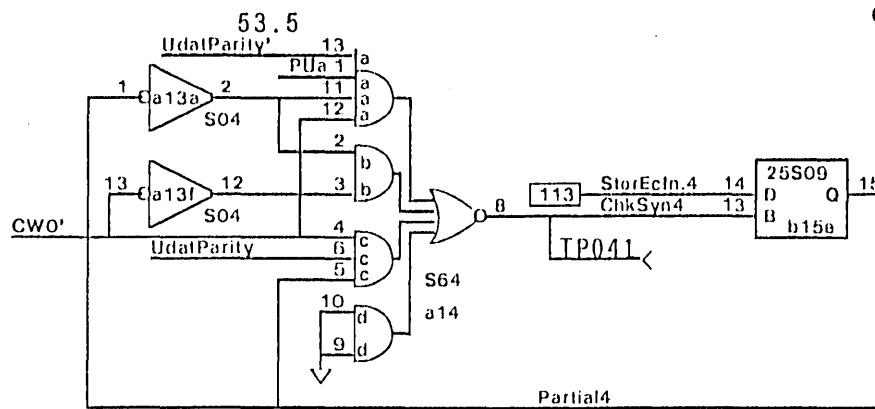


XEROX Project	File	Designer	Rev	Date	Page
EOD DO	DOrnem04.sil	Rosen	Gb	9/19/77	04



XEROX EOD	Project DO	Memory Control Data Paths Bits 08:15	File D0mem05.sil	Designer Rosen	Rev Gb	Date 11/20/77	Page 05
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Note: Storage card inverts data and check bits

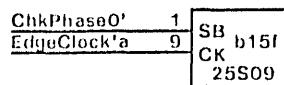
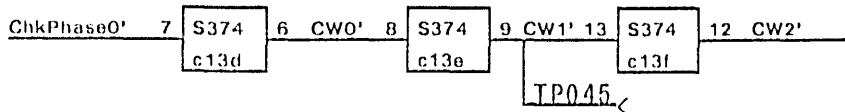
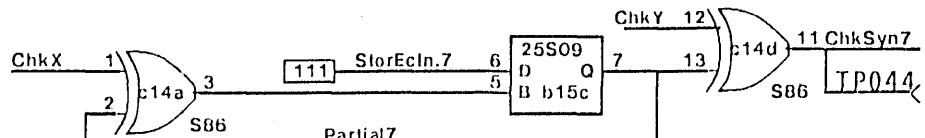


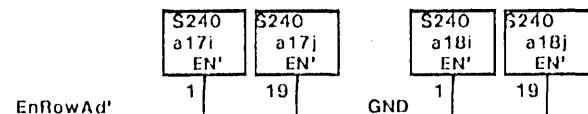
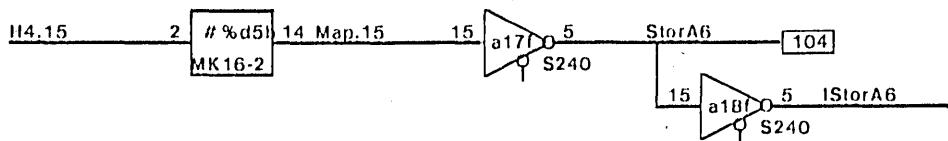
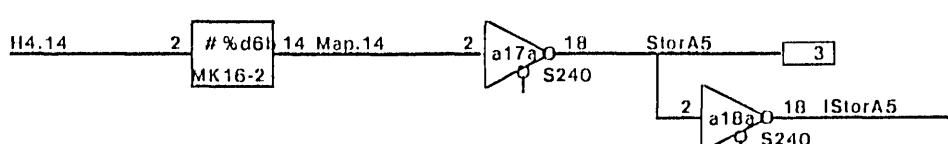
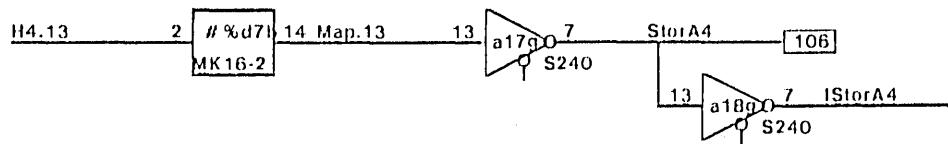
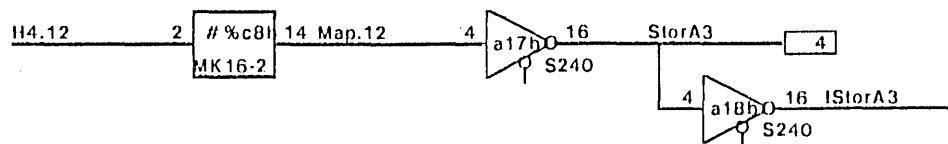
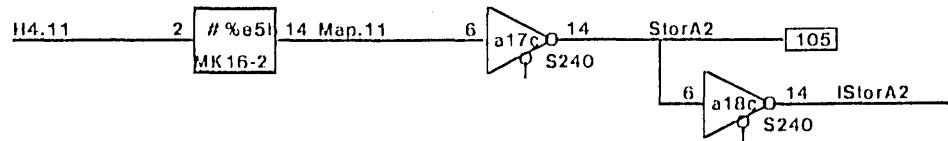
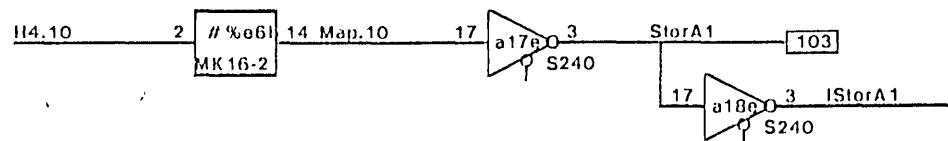
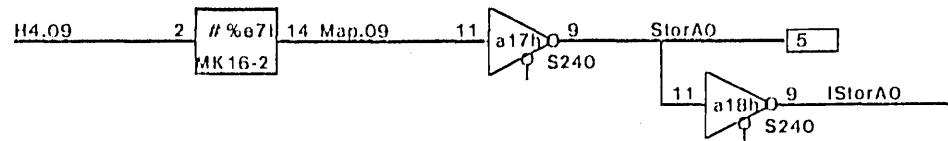
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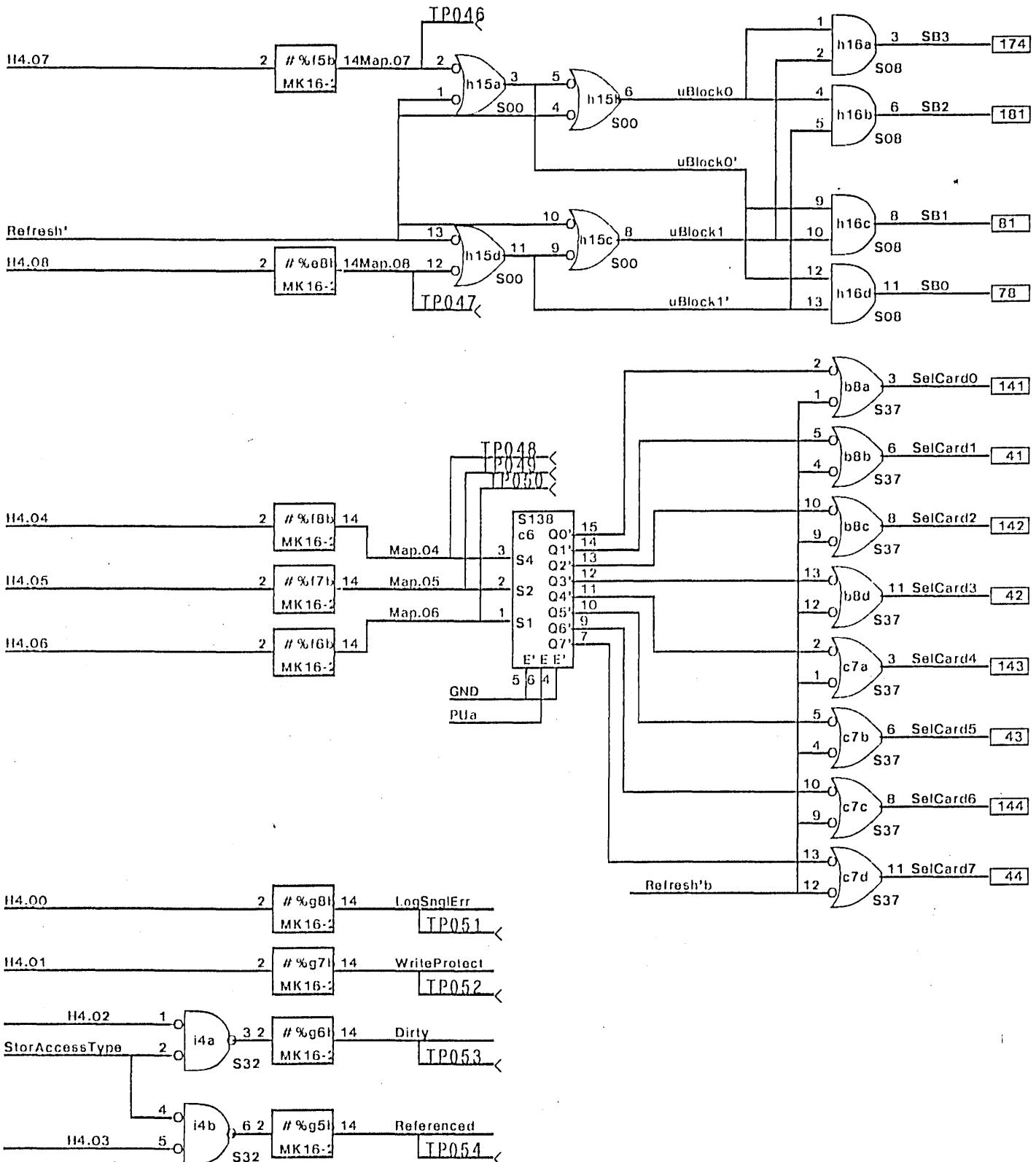
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0	0	0
0	1	1
1	0	1
1	1	0

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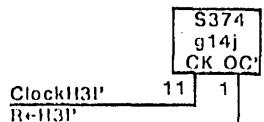
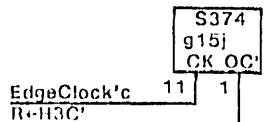
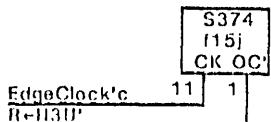
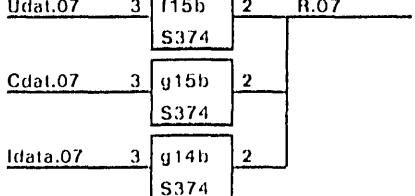
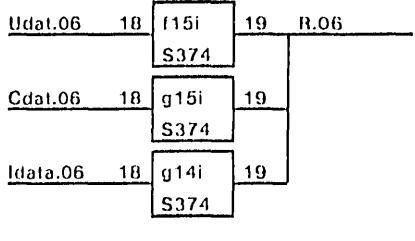
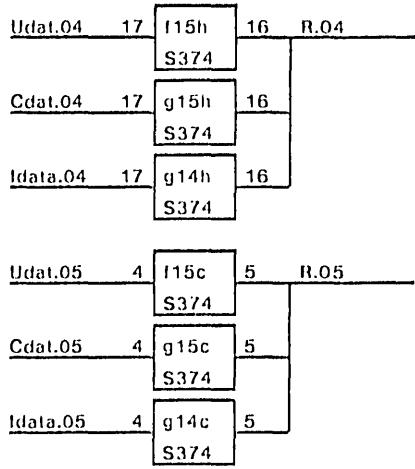
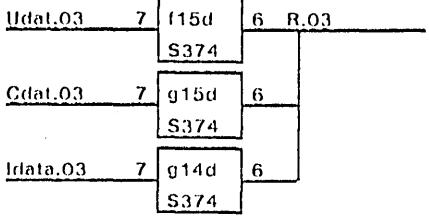
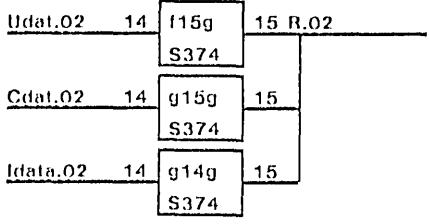
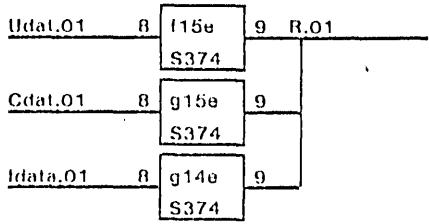
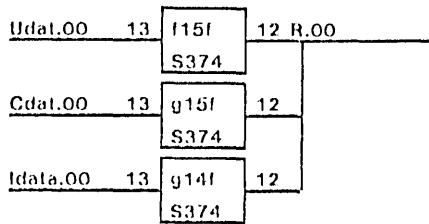
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1	1

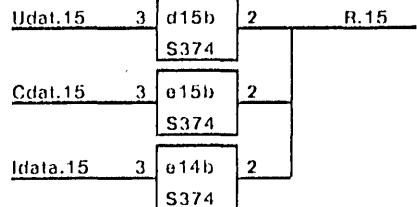
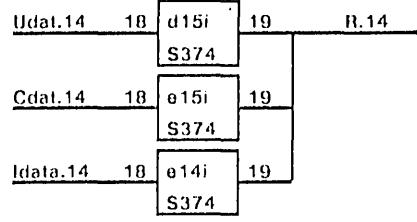
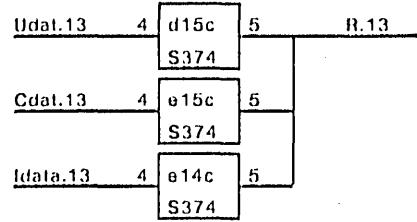
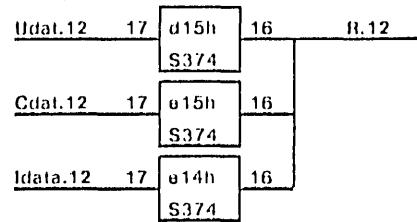
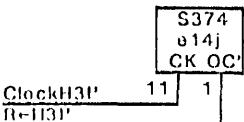
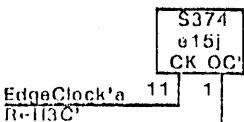
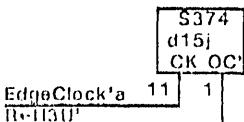
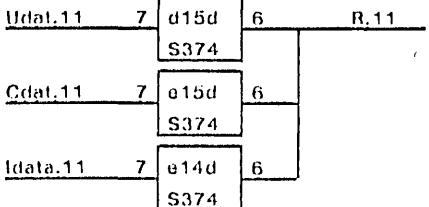
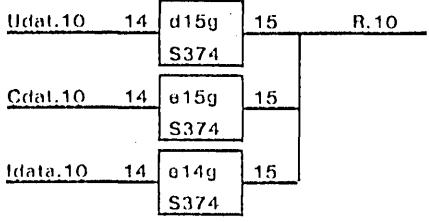
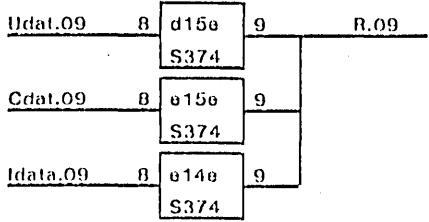
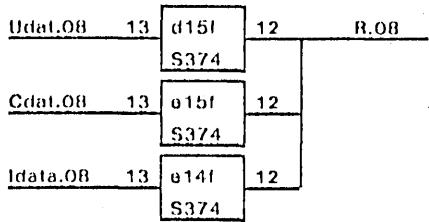




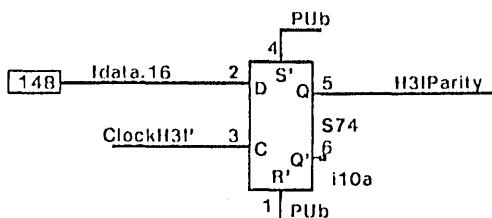
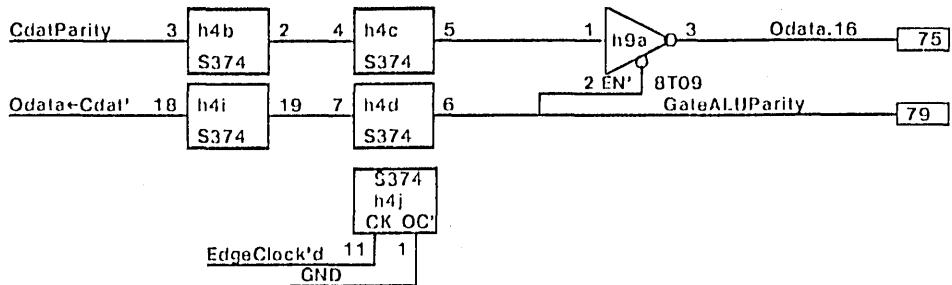


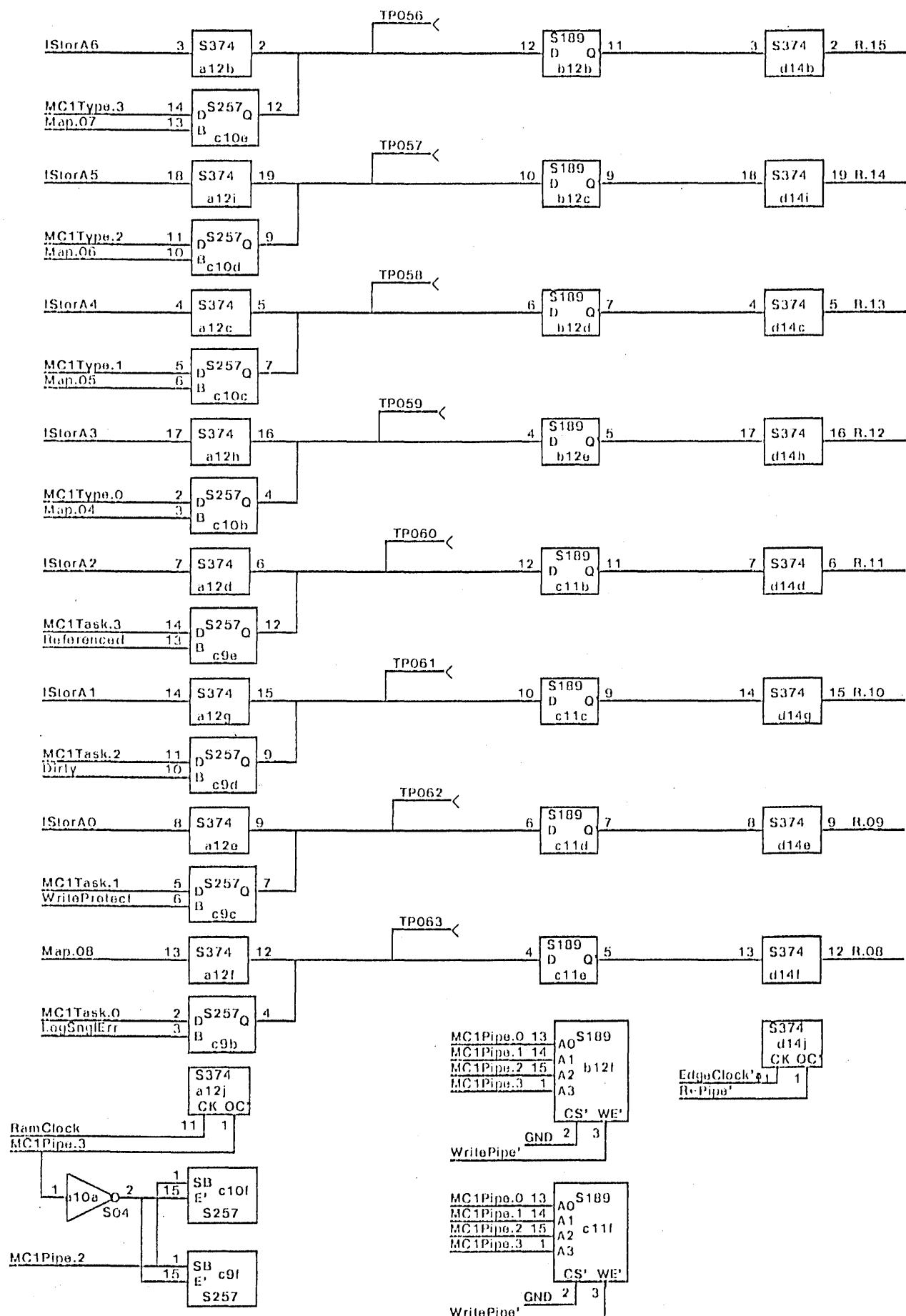
XEROX E0D	Project D0	Memory Control Map A0, Bank, Card, Flags	File D0rnem08.sil	Designer Rosen	Rev Gb	Date 2/19/79	Page 08
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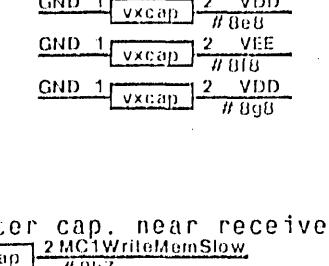
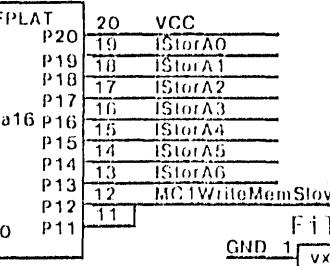
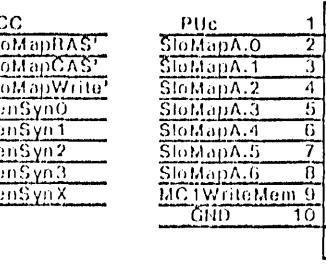
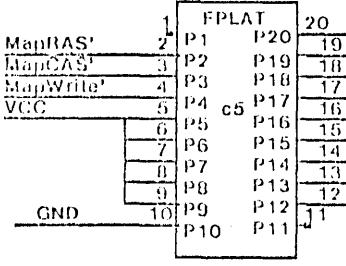
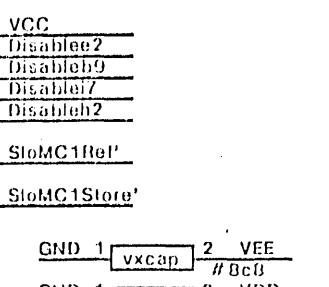
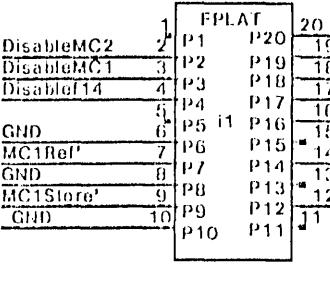
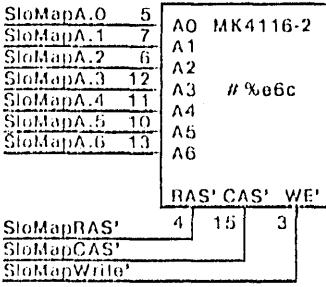
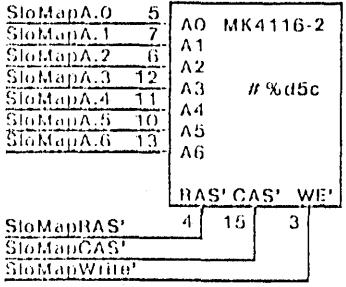
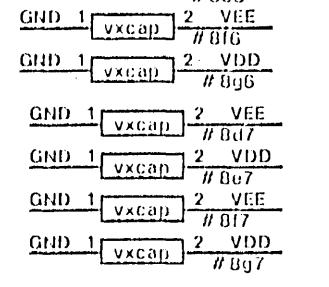
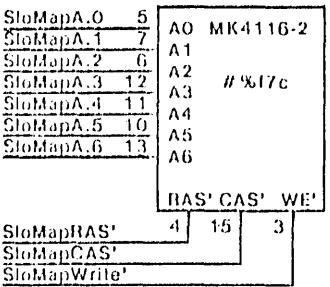
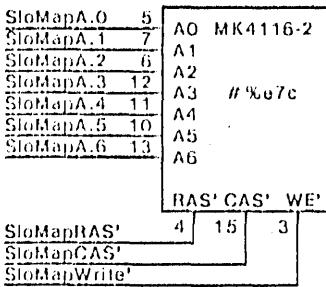
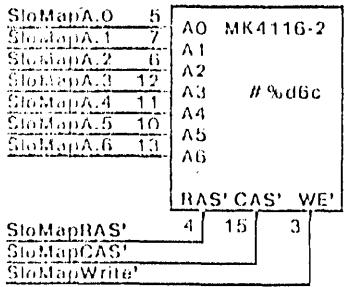
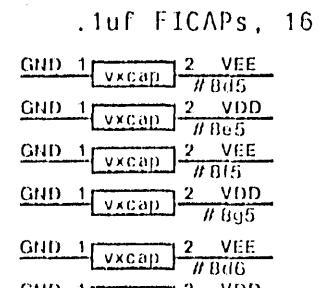
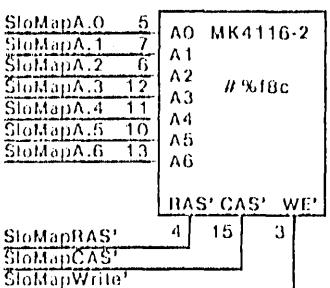
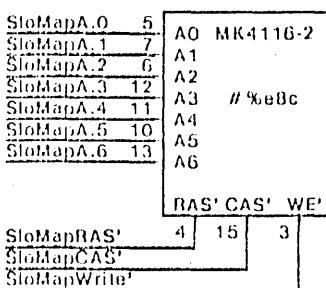
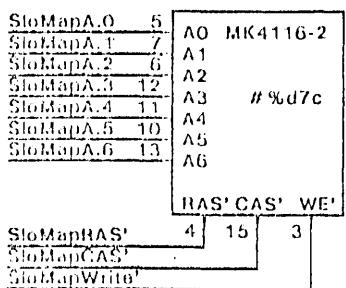
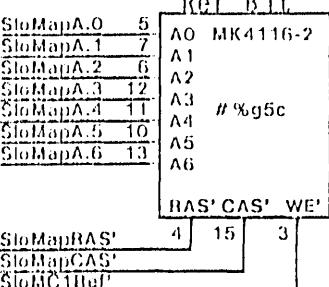
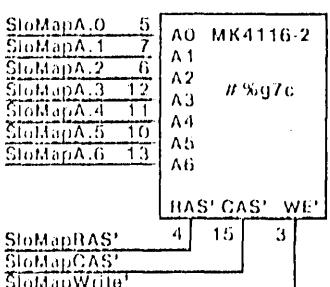
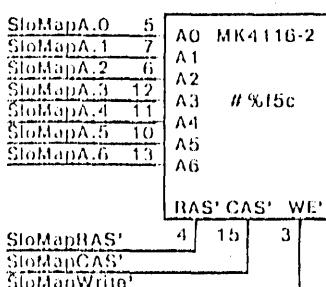
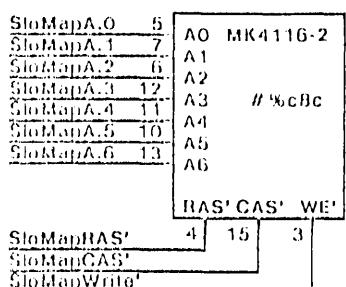
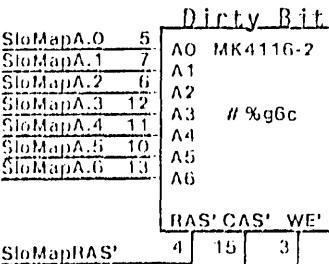
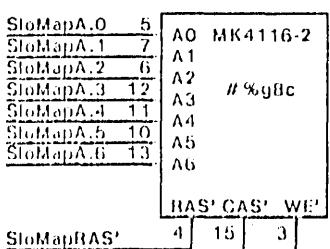
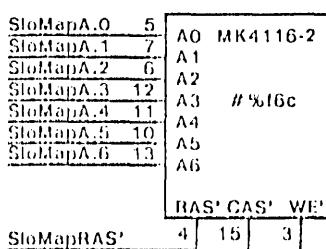
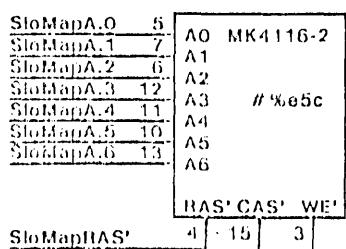


ALU Card supplies parity on OUTPUT





XEROX E0D	Project DO	Memory Control Pipe Data	File D0mem11.sil	Designer Thacker	Rev Gb	Date 5/9/78	Page 11
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Filter cap, near receiver (

GND 1 vxcap 2 VEE # Bc0

GND 1 vxcap 2 VDD # B18

GND 1 vxcap 2 VEE # B18

GND 1 vxcap 2 VDD # Bg6

GND 1 vxcap 2 VEE # B16

GND 1 vxcap 2 VDD # Bg6

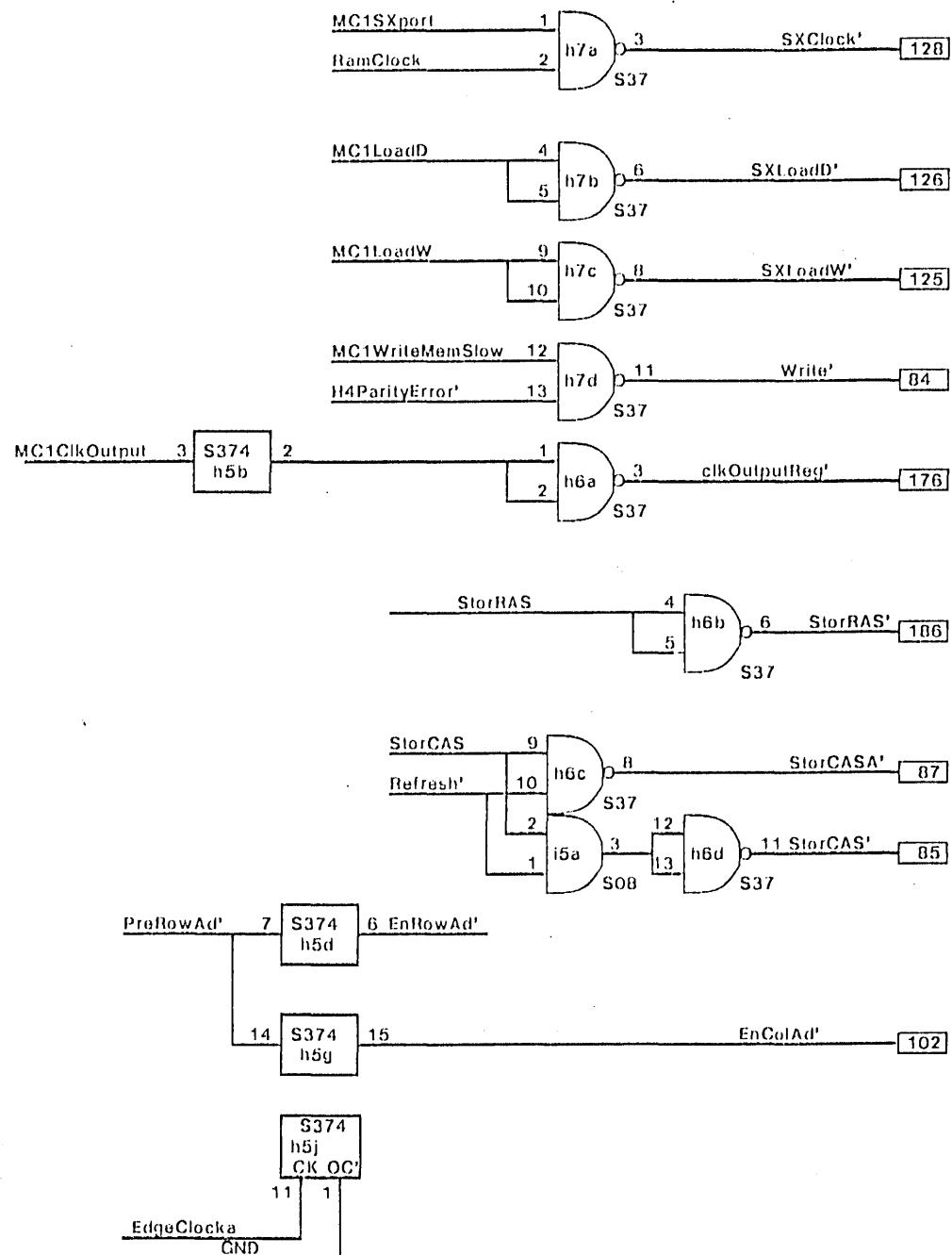
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GND 1 vxcap 2 VDD # Bg7

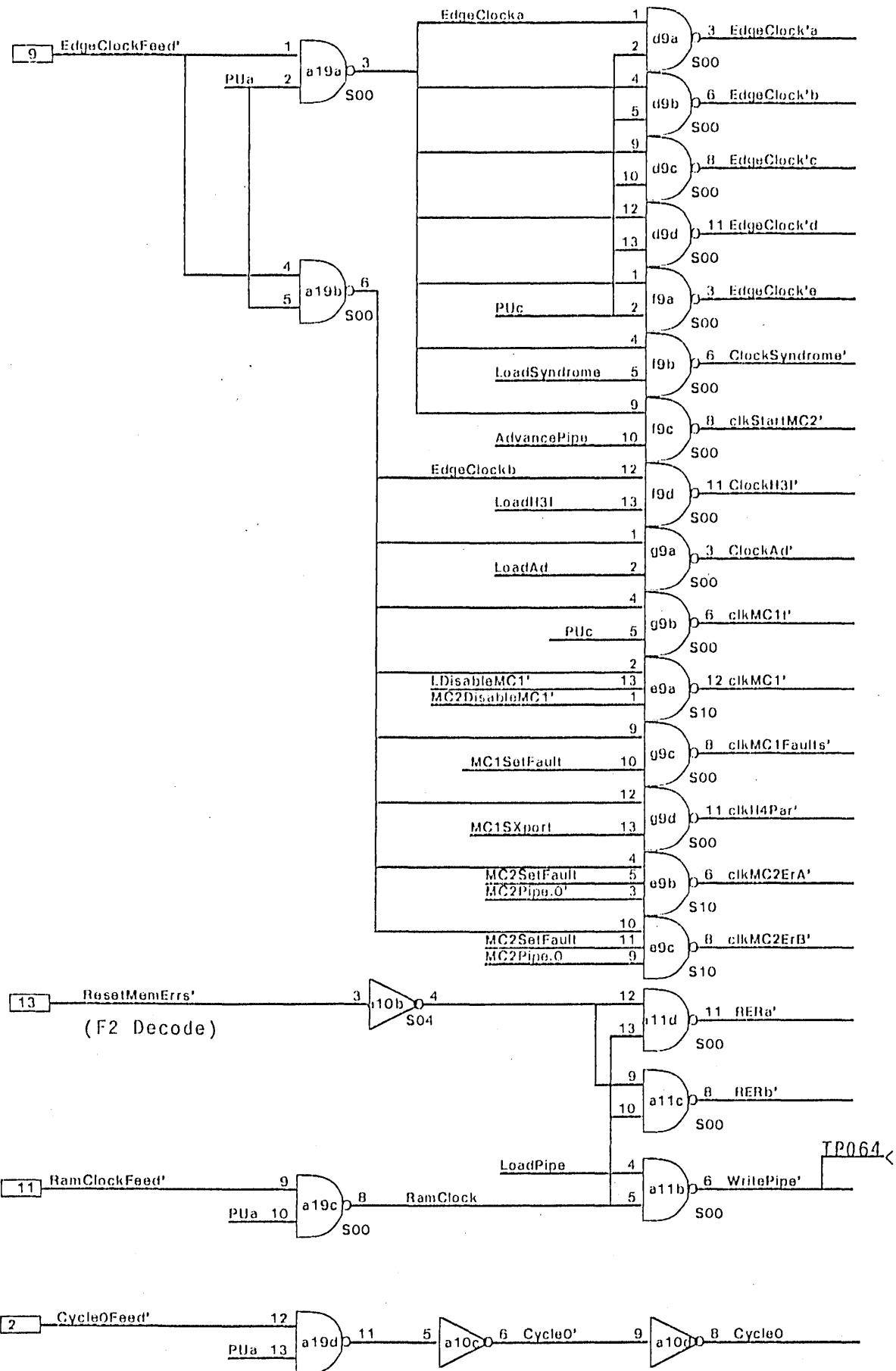
GND 1 vxcap 2 VEE # B17

GND 1 vxcap 2 VDD # Bg7

XEROX	Project	Memory Control	File	Designer	Rev	Date	Page
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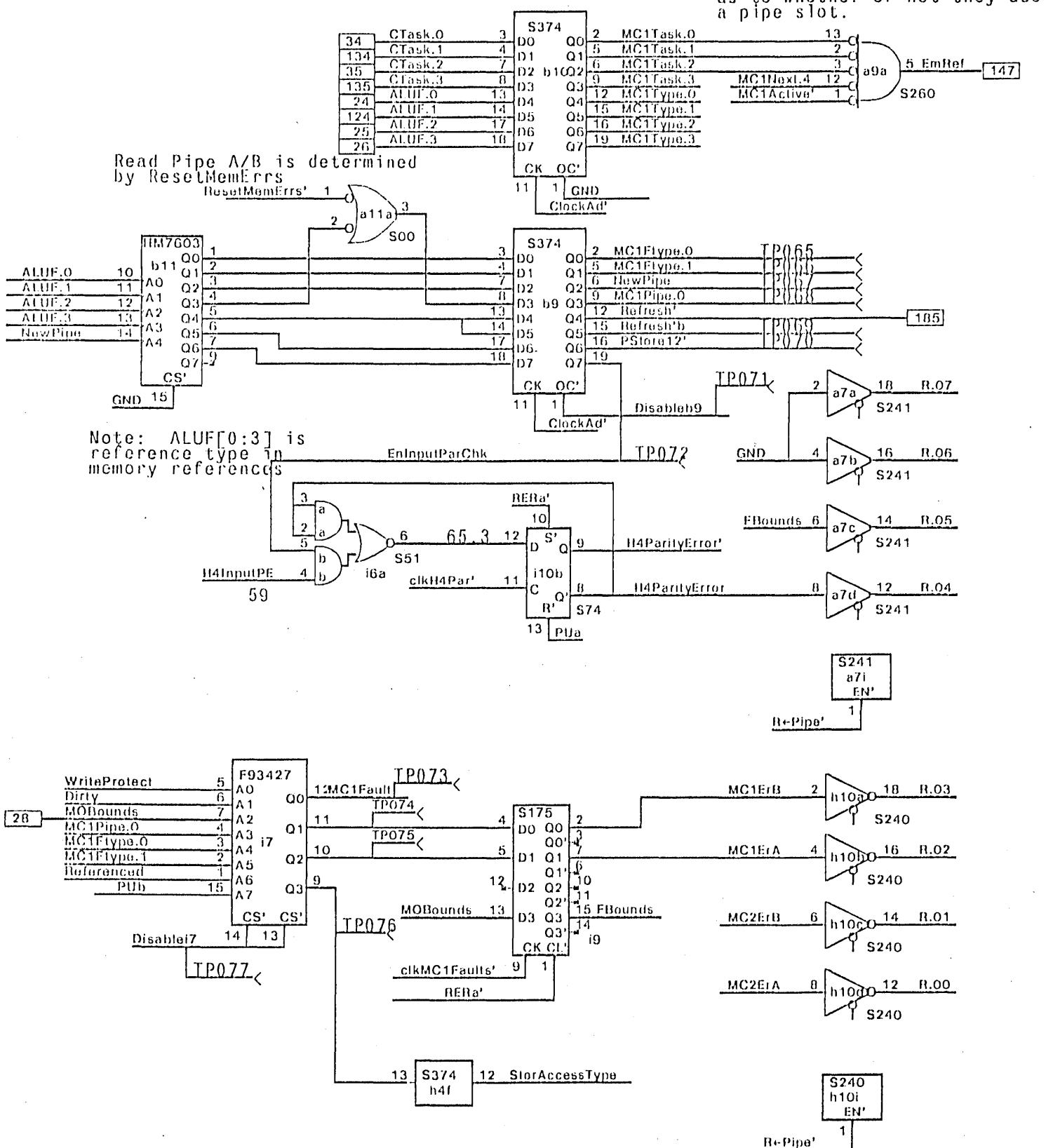
XEROX EOD	Project DO	Memory Control Storage Card Controls	File DOMem13.sil	Designer Thacker	Rev Gb	Date 12/9/78	Page 13
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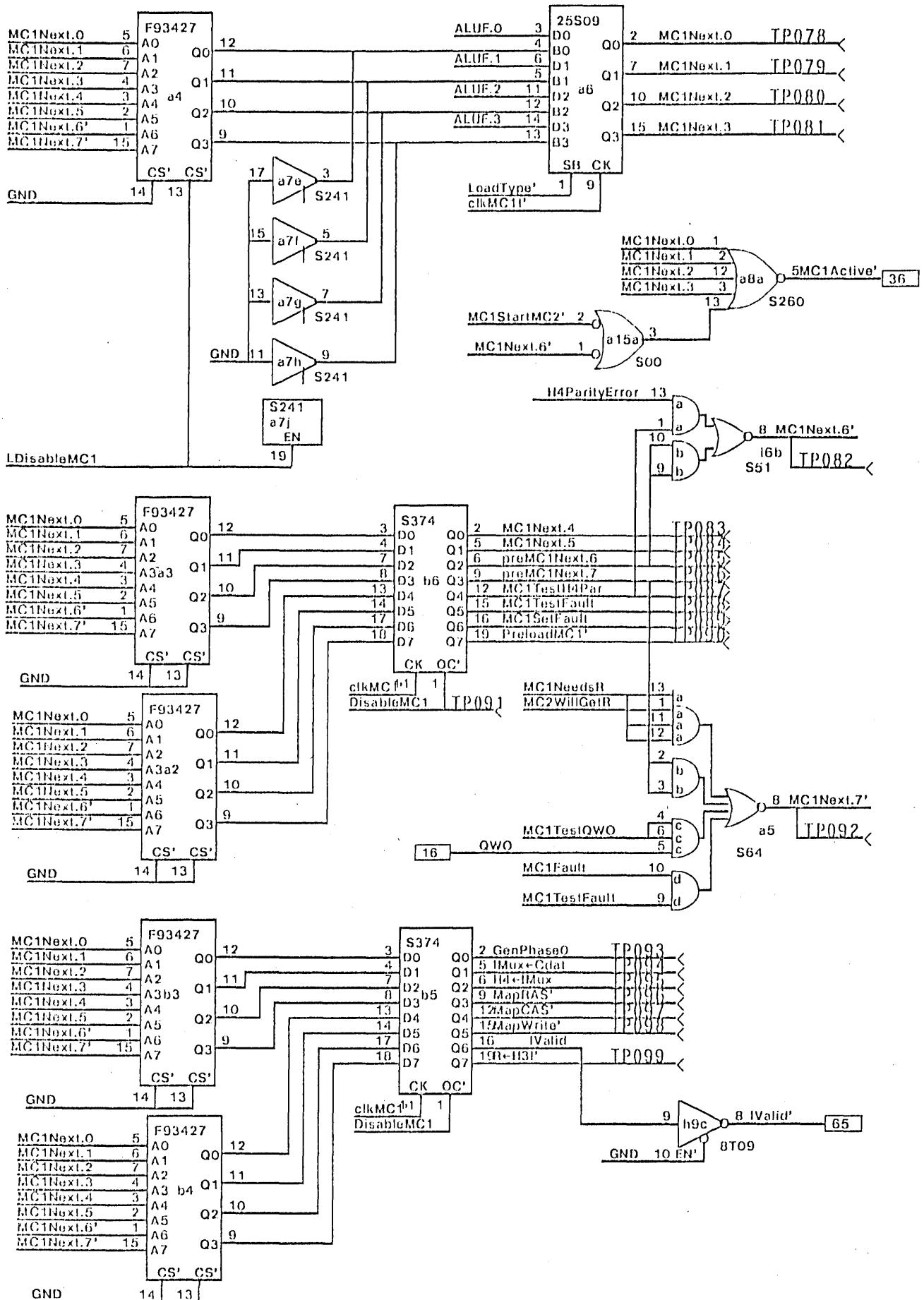


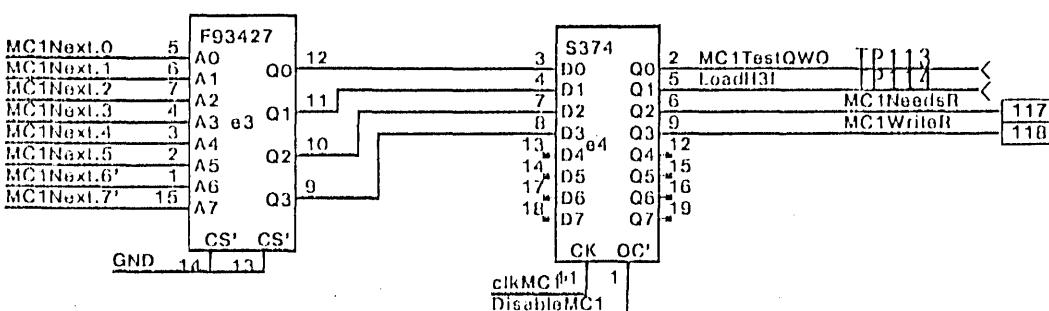
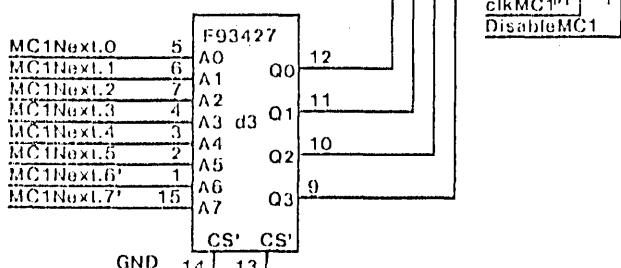
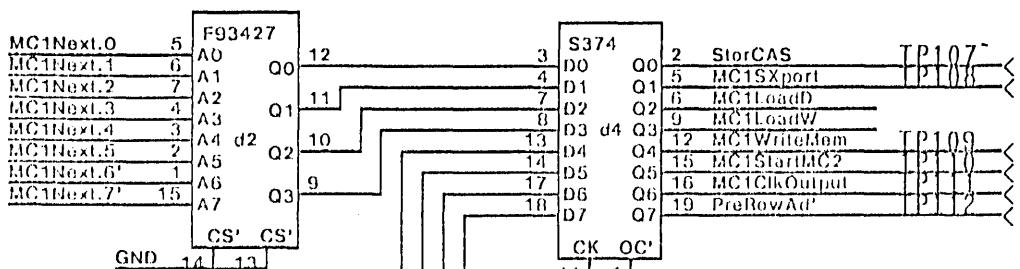
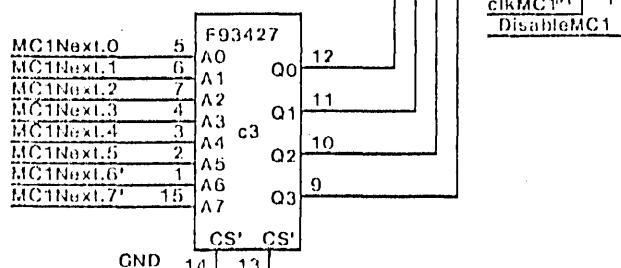
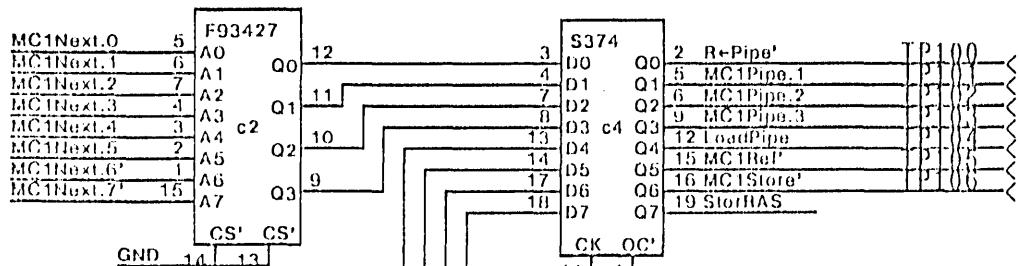
XEROX EOD	Project DO	Memory Control Clocks & Read Mem	File D0mem14.sil	Designer Thacker	Rev Gb	Date 7/18/80	Page 14
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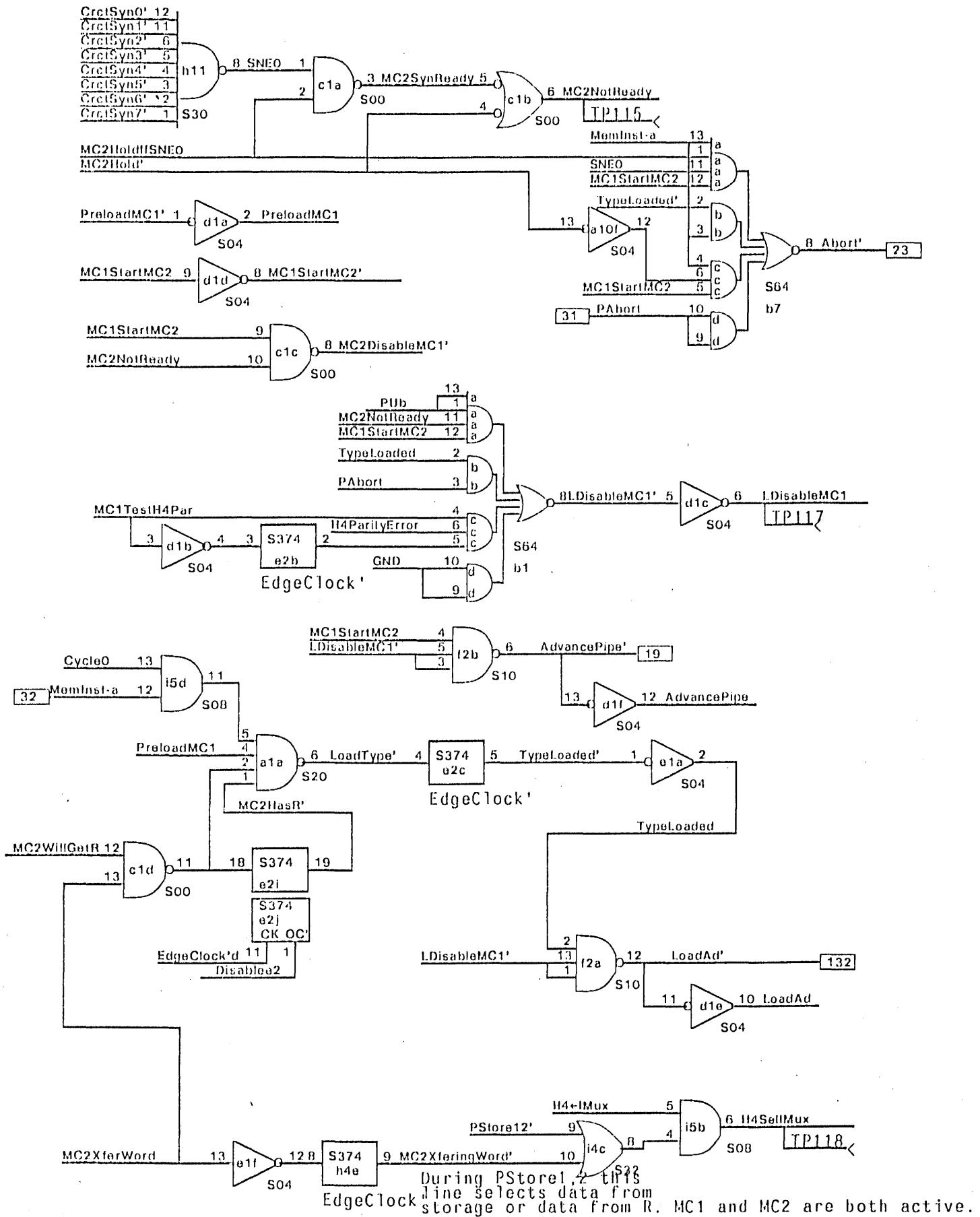
Ftype classifies references according to the types of faults they can cause:  
Non-memory/Fetch/Store

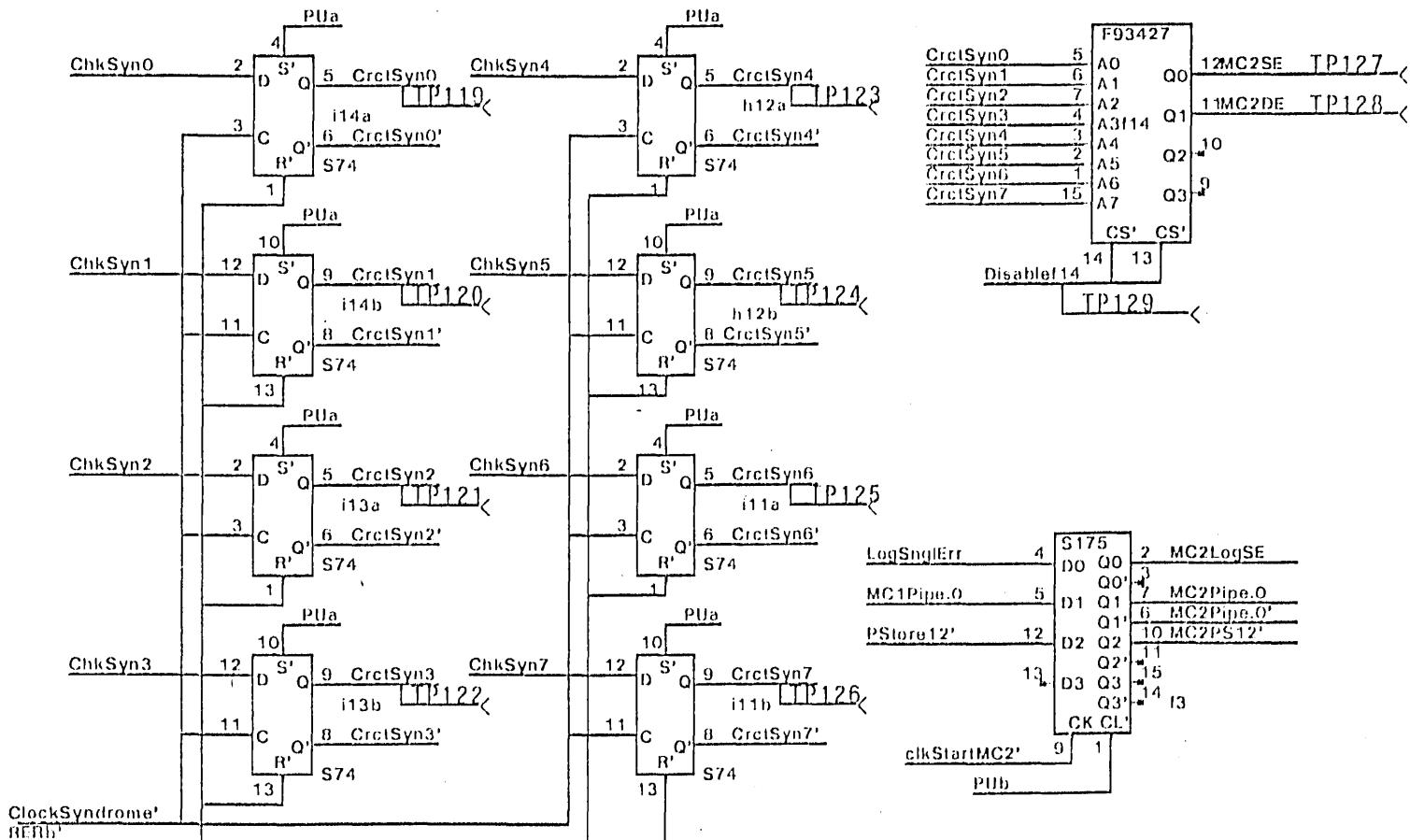
References are also classified as to whether or not they use a pipe slot.









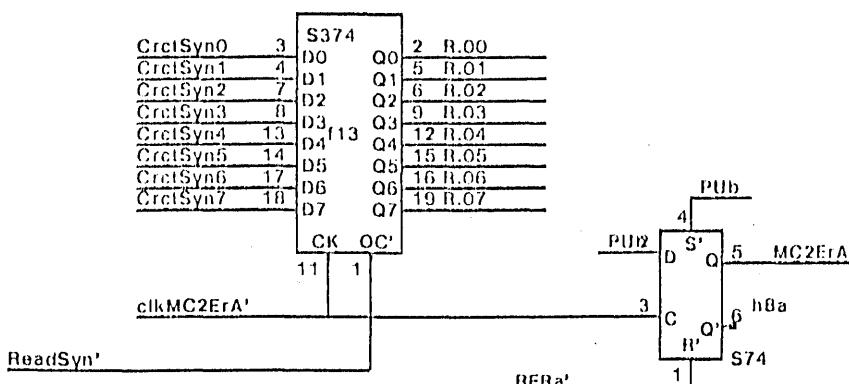


ClockSyndrome'  
RERa'

F93427	5
CrcISyn0	A0
CrcISyn1	A1
CrcISyn2	A2
CrcISyn3	A3
CrcISyn4	A4
CrcISyn5	A5
CrcISyn6	A6
CrcISyn7	A7
CS'	Q3

Disable14  
TP129

S175	2
D0 Q0	3
D1 Q1	4
D2 Q2	5
D3 Q3	6
D4 Q4	7
D5 Q5	8
D6 Q6	9
D7 Q7	10
LogSnglErr	11
MC1Pipe.O	12
PStore12'	13
clkStartMC2'	14
PUIb	15

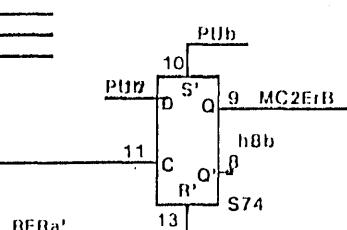


ReadSyn'

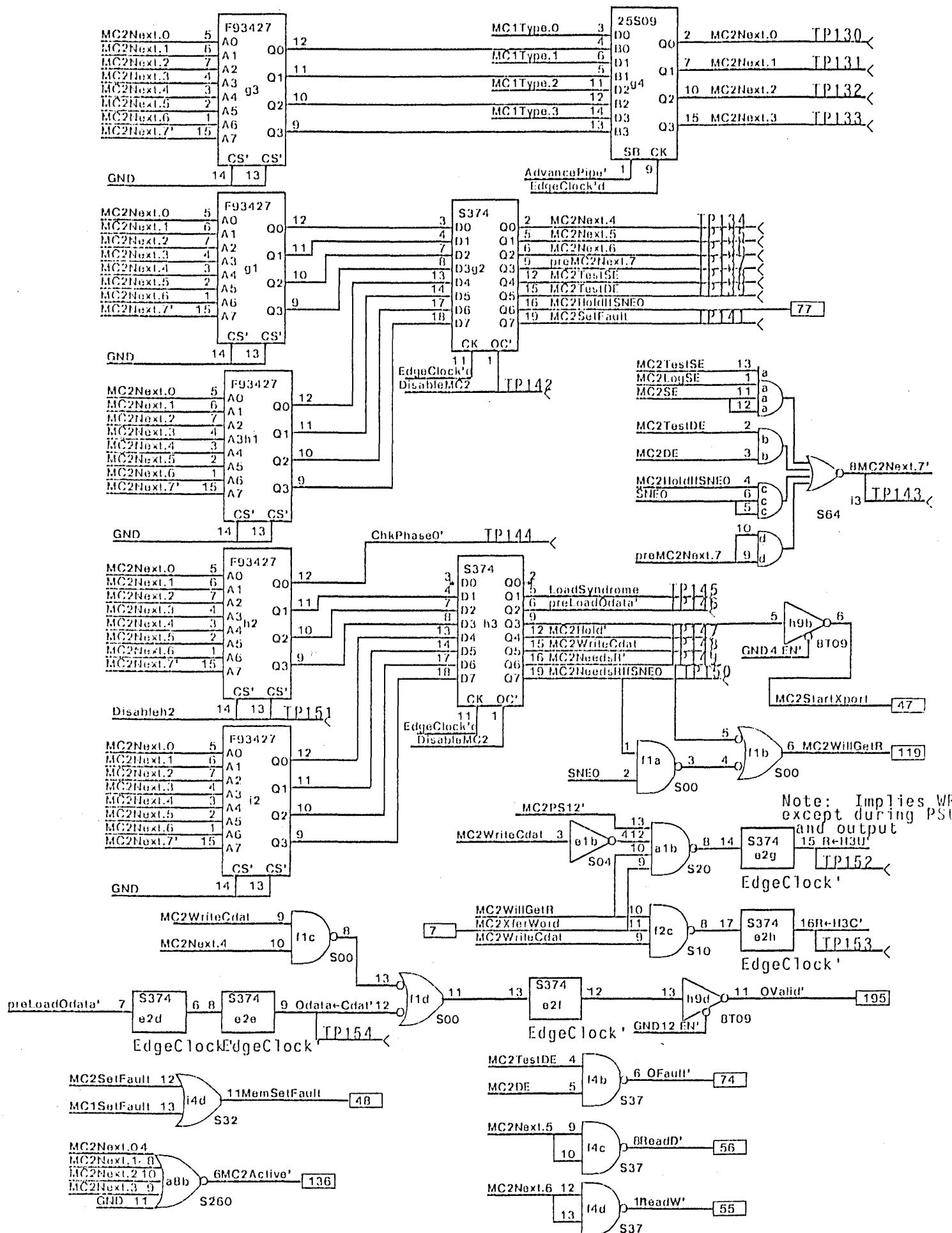
Spare Position

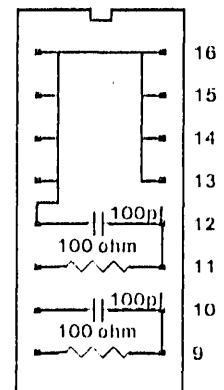
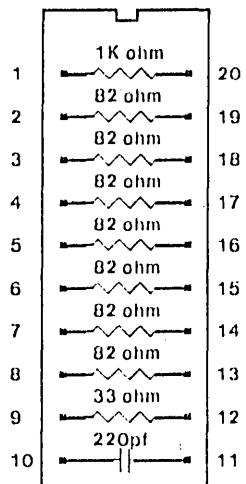
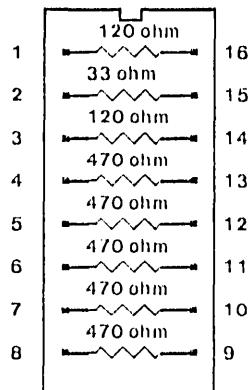
1	FPLAT	20VCC
P1	P20	9
P2	P19	8
P3	P18	7
P4	P17	6
P5b2	P16	5
P6	P15	4
P7	P14	3
P8	P13	2
P9	P12	1
P10	P11	

15 ReadSyn'

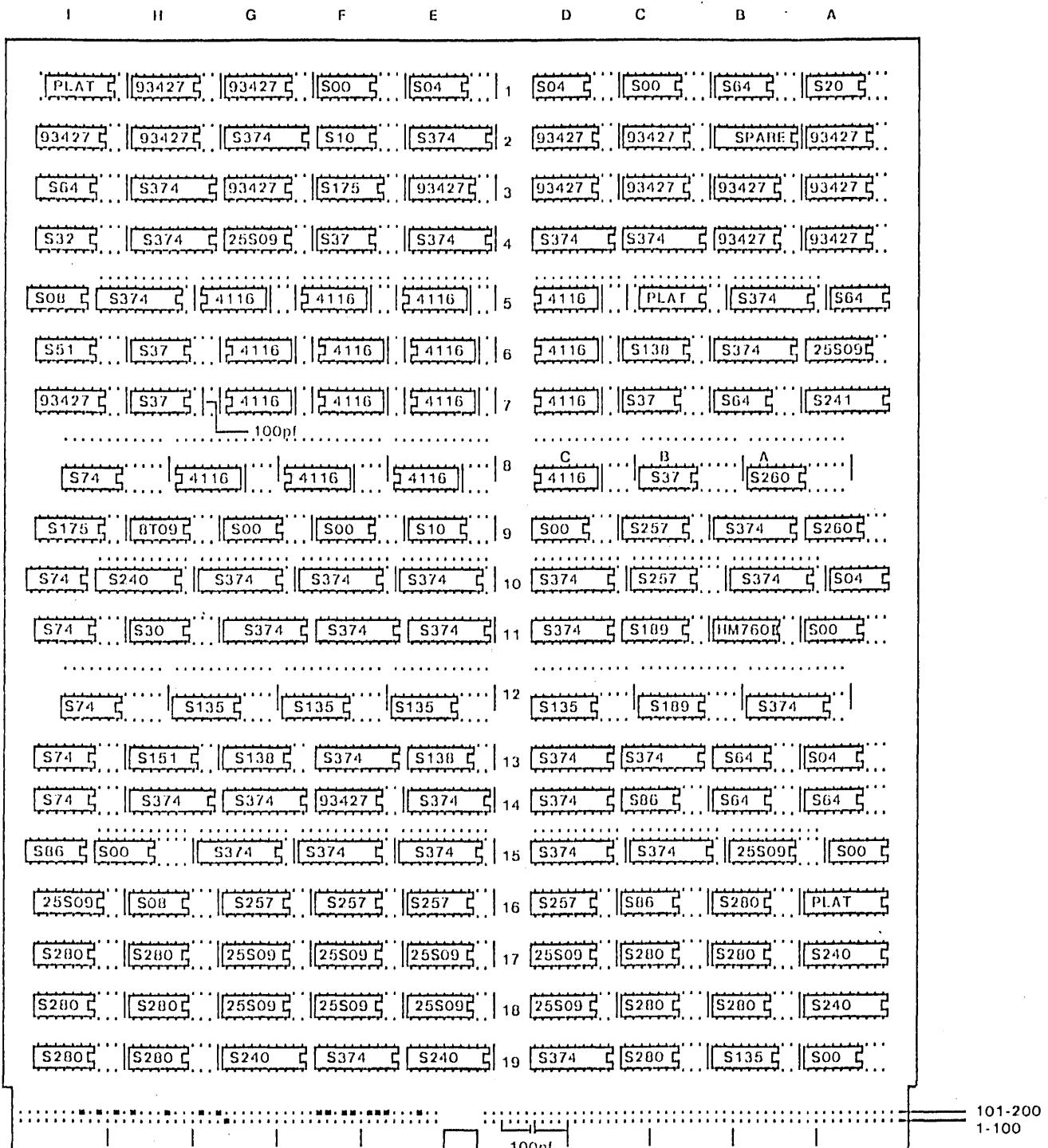


GND



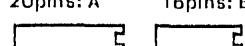


XEROX EOD	Project D0	Memory Control PLATFORMS	File D0MemPLATFORMS.sil	Designer Thacker	Rev Gb	Date 7/18/80
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Note: Pinx marked with ■ have 470ohm pullup resistors to +5v.

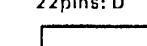
20pins: A



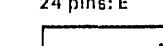
16pins: B



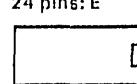
14pins: C



22pins: D



24 pins: E



Note: The short vertical lines indicate  
filler capacitor locations.  
(143 Places)

16pins REVERSED!!!  
typical of MK4116: F



XEROX CSL	Project DD	Memory Control Board Layout	File d0memlayout.sil	Designer Thacker	Rev Gb	Date 7/18/80
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**Changes from Rev E to Rev F:**

- 1) Added the signal Disableb2 (pg 20,12) for test
- 2) Removed H4ParityError' from the term that forms Abort' (gate at a15 now free, inverter at a1a moved).  
Note: This change deletes IC a15.

**Changes from RevF to RevG:**

- 1) b11.15 (pg 1) ← GenX, not GenX' (this was wrong in .nl file, ok on dwg.)
- 2) h13.9 ← CrcSyn4, h13.11 ← CrcSyn6 (pg. 3)

**Changes from RevG to RevH:**

- 1) (pg 13) Change c1.13 from RamClock to EdgeClocka
- 2) (pg 13,15) Changed i9 from S74 to S175. Relocated i9's functions to i10. Added MOBounds as R.05 during R+Pipe operation.
- 3) (pg 16) Deleted S04 at a10e. Replaced with S00 a15a, and added MC1StartMC2' as input to MC1Active.
- 4) Added MC2PS12' by replacing f3 (S74) with S175 (pg 19). MC1PS12' is used instead of PStore12' at a1.13 (pg 20).

**Changes from RevH to RevI (5/9/78)**

- 1) (pg 20) h3.9 was MC2HoldISNEO, is now MC2StartXport' after passing through the BT09 at h9b (used as a driver).
- 2) Renamed signal MC2TestISNEO to MC2HoldISNEO (essentially, these two signals have been coalesced into one).
- 3) Added test points.
- 4) Added comments on Vee bypass and -10V supply changes to D0memplatforms.sil

**Changes from Rev I to Rev J (8/12/78 - C. Thacker)**

- 1) Renamed signal TP055 GateALUParity, and connected it to E079 (pg 10)
- 2) Latched signal StorAccessType in S374 at h4f (pg 15)
- 3) Removed MC2XferWord and MC1XferWord from a5.11 and a5.12. Connected a5.11 and a5.12 to a5.13 (pg 16). Note that signal MC1XferWord is no longer used on this card, so E006 is free.
- 4) Removed -10V supply components on D0memplatforms.sil

**Changes from Rev J to rev K (10/8/78 - C. Thacker)**

- 1) Changed h7.12 from MC1WriteMem to MC1WriteMemSlow (pg13). This signal is generated at platform a16 (pg12).
- 2) Changed platform a16 to 20pins to make room for MC1WriteMemSlow (pg12).
- 3) Added capacitors on SloMapIAS' and SloMapWrite' (platform c5, page 12).
- 4) Changed a9.12 from MC1Task.3 to MC1Next.4 (pg15).
- 5) Changed i7.1 from PUb to Referenced (pg15). This requires changing PROM i7 to revision E.

**Changes from Rev K to rev L (11/1/78 - C. Thacker)**

- 1) Signal clkOutputReg is now clkOutputReg' by removing S37 at h6a (now free) page 13.
- 2) b10.1 (pg15) was Disableb10, is now GND. Also removed Disableb10 from SPLAT i1 (pg 12).

There are no prom changes in this revision.

**Changes from Rev L to rev M (12/9/78 - C. Thacker)**

- 1) Changed platforms c5 and i1 - removed capacitors and changed values.
- 2) Changed the generation of clkOutputReg' (pg 13). This signal is now one cycle wide, rather than being a qualified EdgeClock.
- 3) The input to h5g (pg 13) is PreRowAd', not EnRowAd'. This board requires an ALU board of rev M for proper operation.

There are no prom changes in this revision.

Note: Rev M = Rev Ga

**Changes from rev Ga to rev Gb (7/18/80 - CPT).**

- 1) Added 16 FICAPS for MK4116 chips (VDD and VEE)
- 2) Added glitch suppression capacitor adjacent to h7 (on MC1WriteMemSlow - 100pf).
- 3) Changed interlock logic on page 18.

**Current PROM Revisions:**

a4, a3, a2, b3, b4, c2, c3, d2, d3, e3 (MC1 Sequencer): E

g3, g1, h1, h2, i2 (MC2 Sequencer): D

i7 (Fault): E

b11 (Ftype, Pipe): D

f14 (Single/Double errors): D

XEROX EOD	Project DO	Memory Control Changes	File d0memchanges.sil	Designer Thacker	Rev Gb	Date 7/18/80
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